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Design of an Efficient ALU Using Low-Power Dual Mode Logic

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ABSTRACT
The dual mode logic is an efficient model, which is starts working in between the static and dynamic mode of operations. Since both of the static and dynamic modes having some disadvantages like speed and power dissipations. In this paper we are going to implement a faster and efficient ALU using the DML mode of logic. A performance valuation of designed DML ALU is done with respect to the ordinary normal ALU. And we are implementing this on CADENCE Platform in 180 nm technology. And for a variation of length and width ratio's (W/L) how the design will work is going to be done.

Key words **-** DML-dual mode logic, ALU - arithmetic and logic unit, CPU – central processing unit, GPU – graphical processing unit, MP – microprocessor.

I. INTRODUCTION

In digital electronic systems, an arithmetic and logic unit (ALU) is a digital circuit that performs integer arithmetic operation and logical operations. The ALU [2] is a fundamental building block of the central processing unit (CPU) of a computer, and even the simplest microprocessors (MPs) contain one for needs such as maintaining timers for the timing of the circuitry. The processors found inside modern CPUs and graphics processing units (GPUs) accommodate very powerful and very complex ALUs. A single component may contain a number of ALUs.

Here, in this paper we are using a well known model DML [1] which provides the designer a very high flexibility. As above mentioned DML [1] has overcome the disadvantages of the following two methods – 1) static mode and, 2) dynamic mode. Since, in static mode of operation the power dissipation is low and speed is also very low compared to the dynamic mode. Similarly in dynamic mode the speed is very high and power dissipation is also high compared with static mode.

The objective of this paper is to design an improved in terms of speed especially and an allowable power dissipation. The rest of this paper is having: a review on the DML [1] family explained in the section – II, and in the section –III contains all the implementation of proposed Efficient ALU [2]. And section –IV contains the comparison with the ordinary normal and all the results in terms of power dissipations and speed. Section –V contains the conclusion on the work and future work on this proposal.

II. OVER VIEW OF DML FAMILY

A basic DML gate is having an normal static logic gate, which can be an conventional CMOS logic gate and at the output side we are connecting an normal transistor. And whose gate is connected to a global clock signal is applied to it as switching circuit.

The whole operation is based upon the this external connected transistor and its clock signal speed. The DML can be arranged as two ways depending upon the type of transistor using at the output side either PMOS or NMOS transistor as following way shown in the fig 1.

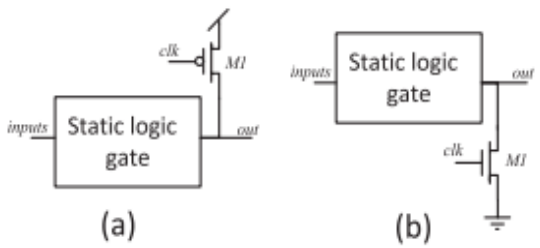

Fig 1: DML topology: (a) type A and (b) type B

As shown in above figure (a) PMOS is connected at the output side and clock is enabled high and similarly in figure (b) at the output side NMOS is connected and clock is enabled low for the switching operations. In above figure (a) when transistor M1 is enabled high the gate is operated in static mode and in figure (b) when transistor M2 is enabled low the gate is again works as normal static mode. But, when the transistor M1 is enabled with clock having both high and low modes then the gate acts as DML gate. Similarly in the type B also in NMOS transistor.

There is an pull-up transistor in type A topology and similarly pull-down transistor in type B topology. Due to this an robust efficiency is achieved

in this DML topologies. Here, the design is operated in two modes of operations based up on the clock signal i.e 1) pre-charge and 2) evaluation modes.

III. PROPOSED ALU

Following fig 2 shows the proposed efficient ALU which can be used in an situation where the systems need an faster operations and the power dissipations are considered up to some extents.

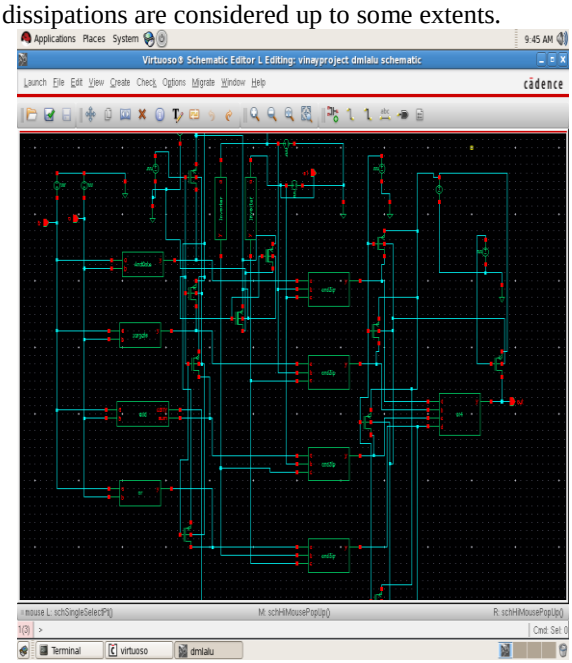

Fig 2: Proposed DML ALU

The above showed figure is the symbol based ALU which is designed in the Cadence Platform by creating symbols to each and every design like OR, HALF ADDER, XOR, and an 1-bit MULTIPLIER gates. For each and every gate at the output side an PMOS gate which is works as an Pull-up circuit in the design.

In our proposed ALU contains the following gates and performs the corresponding operations for an 1-bit inputs. And we can implement them for the 4-bit and 8-bit up to n-bit also.

The logic gates involved in the design are:

1) AND Gate for 1-bit multiplication
2) HALF ADDER
3) XOR Gate
4) OR Gate

And in the multiplexer we are designed four 3-input AND gates, at the output side we are using an 4-input OR Gate in order to select the on of the output in the given 4 –inputs.

IV. FIGURES AND TABLES

In this session we are going to verify the working of the designed DML ALU with respect to the normal ALU in the perspective of power dissipations and speed.

For that we are designed an ordinary normal ALU as same as the our proposed ALU in 1 –bit and going to the their working in all the perspectives like POWER DISSIPATIONS and SPEED in terms of DELAY and also by varying their width in 180 nm technology and also by doing the same in 90 nm technology for the same designs.

The following table- I shows the differences in power dissipation and delay in normal ordinary ALU in 180 nm technology and ALU designed using DML mode.

TABLE I

Power Dissipation and Delay for Different Gate in Normal Mode and DML Mode

S. No	Type of Gate	Normal Mode		DML Mode	
		Pd(pw)	Speed(ns)	Pd(pw)	Delay(ns)
1.	3 IP AND	54	11	53	10
2.	OR	33.14	10	40	9.5
3.	HALF ADDER	159	36	150	33
4.	XOR	94	25	95	23

And also for various sizes of width for NMOS and PMOS in 180 nm technology the power dissipation and delay is verified and the results are verified and the following table II contains the different width of PMOS and NMOS are given.

TABLE II

Power Dissipation and Delay for Different Gate in Normal Mode and DML Mode for different width for PMOS and NMOS.

S. No	Width(um)		Normal Mode		DML Mode	
	PMOS	**NMOS**	**Pd(pw)**	**Delay(ns)**	**Pd(pw)**	Delay(ns)
1.	2	2	376	35	337	**32**
2.	1	1	327	32	275	**30**
3.	1	2	335	30	278	**29**
4.	**2**	**1**	**330**	**28**	**274**	**25**

If the technology parameter changes the power dissipations and delay also changes depending

up on the variation in the length of the transistor. The power dissipation is mainly depends up on the PMOS transistor because the PMOS is directly connected to the VDD. If we reduce the length of the PMOS and NMOS transistor then the power dissipation will be increased since the channel length is main factor in the power dissipation. If we reduce the length the delay will be decreases and consequently the power dissipation will be increases. In the same technology if we reduce the width of the PMOS and NMOS the power dissipation will be optimised up to some extend and delay also be optimised.

Similarly, as we done the same in the 90 nm technology the power dissipation will be gradually increases and the delay will decreases up some range. The schematic of the proposed DML ALU is designed and the power dissipations and delays are verified with respect to the ordinary normal ALU in above said all perspectives. The following fig 3 shows the schematic of DML ALU.

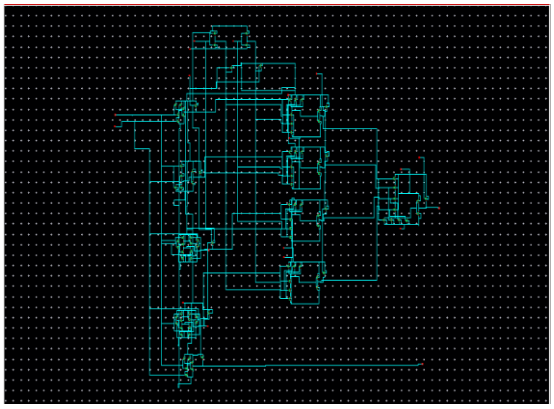

Fig 3: Schematic of DML ALU

We have done the layout for the 3 –input AND gate and also for the 4 –input OR gate using Cadence tool in the 180 nm technology and the layouts are verified and results are also cross checked with the original schematics of the both 4 –input OR gate and 3 –input AND gate. The following fig 4 shows the Layout for the 4 –input OR gate.

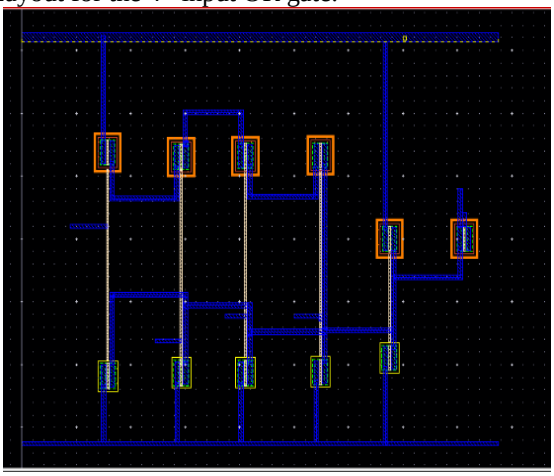

Fig 4: Layout of 4 –input OR gate

And the following fig 5 is the 3 –input AND gate layout and as well as the schematic of the 3 –input AND gate is designed and the results are verified.

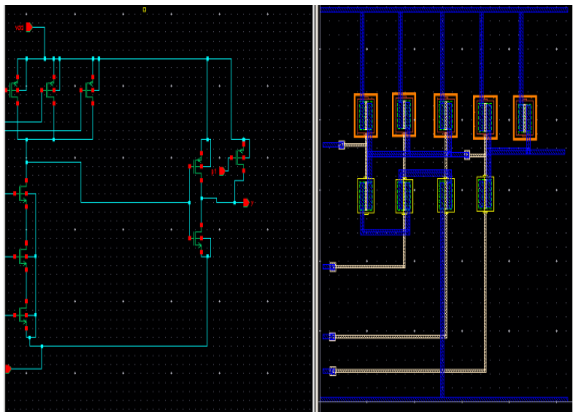

Fig 5: Layout and Schematic of the 3 –input AND gate.

V. CONCLUSION

Dual Mode logic (DML) is the now most popular and advanced logic which is used to for the applications where we need the designs with much faster than the earlier ones. Here in this paper our proposed design of efficient ALU in low power Dual Mode Logic has achieved and an acceptable amount of speed comparing with the earlier logic. This ALU can be extended up to 2, 4, 8..... n bit. Our proposed ALU is designed in Cadence Platform in 180 nm technology. And comparison with the ordinary normal ALU with the designed DML ALU is also done and results are verified. And we have done hoe the design will effect for the variations in the (W/L) i.e the changes of length and width ratio's

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